Dwyer 5-13

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

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| Applicant(s): | Dwyer et al. |
| Case: | 5-13 |
| Serial No.: | 09/975,764 |
| Filing Date: | October 9, 2001 |
| Group: | 2188 |
| Examiner: | John A. Lane |

Title:     Method and Apparatus for Adaptive Cache Frame Locking and Unlocking

## TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

1. Appeal Brief (original and two copies); and

2. Copy of Notice of Appeal, filed on October 13, 2004, with copy of stamped return postcard indicating receipt of Notice by PTO on October 18, 2004.

There is an additional fee of $340 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Deposit Account No. 50-0762** the amount of $340, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter and two copies of the Appeal Brief are enclosed.

Respectfully,

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Date: December 14, 2004

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Patent Application**

5   Applicant(s):   Dwyer et al.
   Case:          5-13
   Serial No.:     09/975,764
   Filing Date:    October 9, 2001
   Group:          2188
10  Examiner:       John A. Lane

> I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450
>
> Signature: *Bobbette Blake* Date: <u>December 14, 2004</u>

Title:   Method and Apparatus for Adaptive Cache Frame Locking and Unlocking

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15   APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

20   Applicants hereby appeal the final rejection dated August 3, 2004, of claims 1 through 36 of the above-identified patent application.

## REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by 25 an assignment recorded on October 9, 2001 in the United States Patent and Trademark Office at Reel 012262, Frame 0653. The assignee, Agere Systems Inc., is the real party in interest.

## RELATED APPEALS AND INTERFERENCES

30   There are no related appeals or interferences.

## STATUS OF CLAIMS

Claims 1 through 36 are pending in the above-identified patent application. Claims 1-36 remain rejected under 35 U.S.C. §103(a) as being unpatentable

over the admitted prior art in view of Malamy et al. (United States Patent Number 5,353,425).

## STATUS OF AMENDMENTS

5      There have been no amendments filed subsequent to the final rejection.

## SUMMARY OF INVENTION

The present invention is directed to a method and apparatus for locking the most recently accessed frames in a cache memory. The most recently accessed frames in

10     a cache memory are likely to be accessed by a task again in the near future. The most recently used frames may be locked at the beginning of a task switch or interrupt to improve the performance of the cache. The list of most recently used frames is updated as a task executes and may be embodied, for example, as a list of frames addresses or a flag associated with each frame. (Page 4, lines 1-30.) The list of most recently used

15     frames may be separately maintained for each task if multiple tasks may interrupt each other. An adaptive frame unlocking mechanism is also disclosed that automatically unlocks frames that may cause a significant performance degradation for a task. The adaptive frame unlocking mechanism monitors a number of times a task experiences a frame miss and unlocks a given frame if the number of frame misses exceeds a

20     predefined threshold. (Page 7, line 12, to page 8, line 5.)

## ISSUES PRESENTED FOR REVIEW

Whether claims 1-36 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of Malamy et al.

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## GROUPING OF CLAIMS

The rejected claims do not stand and fall together. More particularly, for the reasons given below, Applicant believes that each of the dependent claims 5/18, 6/19/24/34, 7/20, 11/21/25/31/35, and 13/27/36 provide independent bases for

30     patentability apart from the rejected independent claims.

## ARGUMENT

Independent claims 1, 15, 23, and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of Malamy et al.

In particular, the Examiner asserts that the admitted prior art teaches the
5 claimed step of "locking frames if a task is interrupted by another task." The Examiner acknowledges that the admitted prior art does not discuss locking a frame or frames in accordance with a most recently used scheme, but asserts that Malamy teaches locking pages or blocks in the cache in accordance with a most recently used locking scheme.

First, Applicants note that the admitted prior art teaches to lock all frames
10 associated with a task, if the task is interrupted by another task. Independent claims 1 and 29 require locking a number of most recently used frames *associated with a task.* Independent claims 15 and 23 require locking said number of said most recently used frames *if a task is interrupted by another task.* Thus, the admitted prior art actually *teaches away* from the present invention by teaching to lock *all* frames associated with a
15 task.

Applicants also note that Malamy teaches a scheme that prevents the most recently used lines in a cache from being replaced when the cache controller is forced to replace a cache memory line. The most recently used cache lines are thus blocked from being replaced, *regardless of the task they are associated with and regardless of whether*
20 *a task is interrupted by another task.* The present invention, alternatively, recognizes that the most recently accessed frames in a cache memory are likely to be accessed by a task again in the near future. Thus, the most recently used frames *associated with a task* may be locked in accordance with the present invention at the beginning of a task switch or interrupt, and are thus available when an interrupted task resumes execution (to improve
25 the performance of the cache. Independent claims 1 and 29 require locking a number of most recently used frames *associated with a task.* Independent claims 15 and 23 require locking said number of said most recently used frames *if a task is interrupted by another task.* Malamy, therefore, actually *teaches away* from the present invention by teaching to block the replacement of the most recently used cache lines *regardless of the task they*
30 *are associated with.*

Conclusion

Thus, the admitted prior art and Malamy, alone or in combination, do not disclose or suggest locking a number of most recently used frames associated with a task, as required by independent claims 1 and 29, and do not disclose or suggest locking said number of said most recently used frames if a task is interrupted by another task, as required by independent claims 15 and 23. Furthermore, Applicants could find no disclosure or suggestion in the prior art to combine the prior art techniques cited by the Examiner and, as stated above, each of the cited prior art disclosures actually teaches away from the present invention. Thus, a person of ordinary skill in the art would not look to combine Malamy and the admitted prior art.

The rejections of the independent claims under section §103 in view of the admitted prior art and Malamy are therefore believed to be improper and should be withdrawn.

Dependent Claims

Claims 5/18, 6/19/24/34, 7/20, 11/21/25/31/35, and 13/27/36 specify a number of limitations providing additional bases for patentability. Specifically, the Examiner rejected claims 5 and 18 under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of Malamy et al. Claims 5 and 18 require an identifier of the n most recently used frames is maintained for each of a plurality of tasks. Claims 6, 19, 24, and 34 require not locking all the frames in a set concurrently. Claims 7 and 20 require wherein said number of said most recently used frames identifies the most recently accessed 3n/2 frames on average. Claims 11, 25, 31, and 35 require an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task. Claims 13 and 36 require wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

Regarding the dependent claims, the Examiner asserts that it is believed that most, if-not-all, dependent claim features are taught by the admitted prior art and/or Malamy.

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The admitted prior art and Malamy (alone or in combination), however, do not disclose or suggest an identifier of the n most recently used frames is maintained for each of a plurality of tasks, as required by claims 5 and 18, do not disclose or suggest not locking all the frames in a set concurrently, as required by claims 6, 19, 24, and 34, do

5    not disclose or suggest wherein said number of said most recently used frames identifies the most recently accessed 3n/2 frames on average, as required by claims 7 and 20, do not disclose or suggest an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task, as required by claims 11, 25, 31, and 35, and do not disclose or suggest wherein said cache is a two way set associative

10    cache and said most recently used frames are identified by taking an inverse of a least recently used identifier, as required by claims 13 and 36.

The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is

15    appreciated.

Respectfully,

20    Date: December 14, 2004          Kevin M. Mason
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## APPENDIX

1.   A cache memory, comprising:

   a plurality of cache frames for storing information from main memory; and

   an adaptive frame locking mechanism for locking a number of most recently used frames associated with a task.

2.   The cache memory of claim 1, further comprising a memory for recording an identifier of the n most recently used frames.

3.   The cache memory of claim 2, wherein said identifier is a frame address.

4.   The cache memory of claim 2, wherein said identifier is a flag associated with said most recently used frames.

5.   The cache memory of claim 2, wherein said identifier of the n most recently used frames is maintained for each of a plurality of tasks.

6.   The cache memory of claim 1, wherein said adaptive frame locking mechanism does not lock all the frames in a set concurrently.

7.   The cache memory of claim 1, wherein said number of said most recently used frames identifies the most recently accessed 3n/2 frames on average.

8.   The cache memory of claim 1, wherein said adaptive frame locking mechanism includes three latches (a, b, and lock) for each frame of said cache.

9.   The cache memory of claim 8, wherein said latch a is set when a frame is accessed and the value in latch a of a frame is transferred to latch b and latch a is reset after n accesses.

10.     The cache memory of claim 8, wherein said adaptive frame locking mechanism sets a lock latch of a given frame, locking the frame, if either latch a or latch b is set when the lock signal is asserted.

5   11.     The cache memory of claim 1, further comprising an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task.

12.     The cache memory of claim 11, wherein said adaptive frame unlocking
10  mechanism includes a counter for monitoring a number of times a task experiences a frame miss.

13.     The cache memory of claim 1, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse
15  of a least recently used identifier.

14.     The cache memory of claim 1, wherein said locking is performed if a first task is interrupted by a second task.

20  15.     A method for locking frames in a cache memory, said method comprising the steps of:
        storing information from main memory in frames of said cache memory;
        monitoring a number of most recently used frames; and
        locking said number of said most recently used frames if a task is
25  interrupted by another task.

16.     The method of claim 15, wherein said monitoring step maintains a frame address of said most recently used frames.

30  17.     The method of claim 15, wherein said monitoring step maintains a flag associated with said most recently used frames.

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18.        The method of claim 15, wherein said monitoring step maintains an identifier of the n most recently used frames for each of a plurality of tasks.

19.        The method of claim 15, wherein said locking step does not lock all the
5    frames in a set concurrently.

20.        The method of claim 15, wherein said number of said most recently used frames identifies the most recently accessed $3n/2$ frames on average.

10    21.        The method of claim 15, further comprising the step of automatically unlocking frames that cause a significant performance degradation for a task.

22.        The method of claim 21, wherein said step of unlocking further comprises the step of monitoring a number of times a task experiences a frame miss.

15

23.        A cache memory comprising:
          a memory element for storing information from main memory in frames of said cache memory;
          means for monitoring a number of most recently used frames; and
20         means for locking said number of said most recently used frames if a task is interrupted by another task.

24.        The cache memory of claim 23, wherein said means for locking said frames does not lock all the frames in a set concurrently.

25

25.        The cache memory of claim 23, further comprising means for unlocking said locked frames that automatically unlocks frames that cause a significant performance degradation for a task.

30    26.        The cache memory of claim 25, wherein said means for unlocking includes a counter for monitoring a number of times a task experiences a frame miss.

27.     The cache memory of claim 23, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

5      28.     The cache memory of claim 23, wherein said locking is performed if a first task is interrupted by a second task.

29.     An integrated circuit, comprising:

        a cache memory having a plurality of cache frames for storing information

10    from main memory; and

        an adaptive frame locking mechanism for locking a number of most recently used frames associated with a task.

30.     The integrated circuit of claim 29, further comprising a memory for

15    recording an identifier of the n most recently used frames.

31.     The integrated circuit of claim 29, further comprising an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task.

20

32.     The integrated circuit of claim 29, wherein said locking is performed if a first task is interrupted by a second task.

33.     A cache memory device comprising:

25            a memory element for storing information from main memory in frames of said cache memory device;

        a monitor for monitoring a number of most recently used frames; and

        an adaptive frame locking mechanism for locking said number of said most recently used frames if a task is interrupted by another task.

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34.      The cache memory device of claim 33, wherein said adaptive frame locking mechanism does not lock all the frames in a set concurrently.

35.      The cache memory device of claim 33, wherein said adaptive locking mechanism automatically unlocks frames that cause a significant performance degradation for a task.

36.      The cache memory device of claim 33, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

12/21/04

# ⒸCOPY

| **NOTICE OF APPEAL** FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES | Docket Number (Optional) Dwyer 5-13 |
|---|---|

| I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Assistant Commissioner for Patents, Washington D.C. 20231" on **October 13, 2004** . <br><br> Signature _____. <br> Typed or printed name **Tina Maurice** | In re Application of <br> **Dwyer et al.** |
|---|---|

| | Application Number | Filed |
|---|---|---|
| For **Method and Apparatus for Adaptive Cache Frame Locking and Unlocking** | 09/975,764 | October 9, 2001 |

| | Group Art Unit | Examiner |
|---|---|---|
| | 2188 | John A. Lane |

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 1.17(b))          $ 340.00 .

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is:          $_____.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Commissioner has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.

☑ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No._____50-0762_____. I have enclosed a duplicate copy of this sheet.

☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record.

☐ attorney or agent acting under 37 CFR 1.34(a). Registration number if acting under 37 CFR 1.34(a)._____.

*Kevin M. Mason*
Signature

Kevin M. Mason
Typed or printed name

October 13, 2004
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

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**FAIRFIELD, CT 06824**

Receipt in the USPTO is hereby acknowledged of:

Transmittal Letter – (Original & 1 copy)
Notice of Appeal - (Original & 1 copy)

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Case Name: Dwyer 5-13
Serial No.: 09/975,764

1150-1025

October 13, 2004  KMM